RC5051

Programmable Synchronous DC-DC Converter for Low Voltage Microprocessors

Features

- Programmable output from 1.3V to 3.5V using an integrated 5-bit DAC
- 85% efficiency typical
- Adjustable operation from 80KHz to 1MHz
- Integrated Power Good and Enable functions
- Overvoltage protection
- Short circuit protection with current limiting
- Drives N-channel MOSFETs
- 20 pin SOIC package
- Meets Intel Pentium II specifications using minimum number of external components

Applications

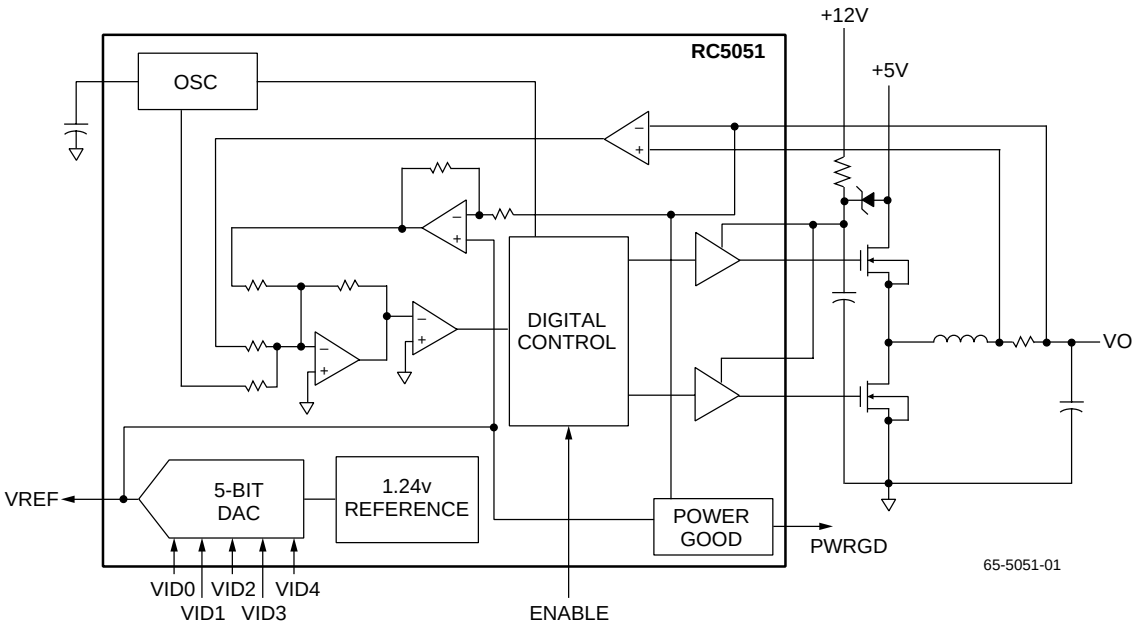
- Power supply for Pentium II
- VRM for Pentium II processor
- Programmable step-down power supply

Description

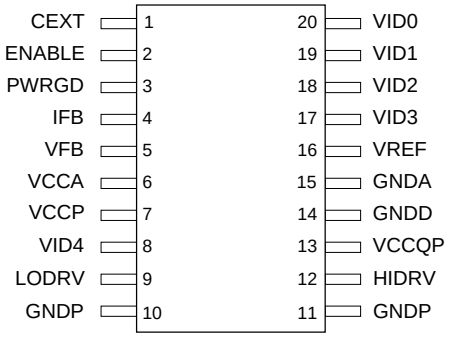
The RC5051 is a synchronous mode DC-DC controller IC which provides an accurate, programmable output voltage for all Pentium II CPU applications. The RC5051 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5051 uses a high level of integration to deliver load currents in excess of 17A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range, and the internal oscillator can be programmed from 80KHz to 1MHz for additional flexibility in choosing external components. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5051 also offers integrated functions including Power Good, Output Enable, over-voltage protection and current limiting.

Preliminary Information

Block Diagram



Pin Assignments



Preliminary Information

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	CEXT	**Oscillator Capacitor Connection**. Connecting an external capacitor to this pin sets the internal oscillator frequency. Layout of this pin is critical to system performance. See Application Information for details.
2	ENABLE	**Output Enable**. A logic LOW on this pin will disable the output. An internal pull-up resistor allows for either open collector or TTL compatibility.
3	PWRGD	**Power Good Flag**. An open collector output that will be at logic LOW if the output voltage is not within ±12% of the nominal output voltage setpoint.
4	IFB	**High Side Current Feedback**. Pins 4 and 5 are used as the inputs for the current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
5	VFB	**Voltage Feedback**. Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. See Application Information for details regarding correct layout.
6	VCCA	**Analog VCC**. Connect to system 5V supply and decouple with a 0.1µF ceramic capacitor.
7	VCCP	**Power VCC for low side FET driver**. Connect to system 5V supply and place a 4.7µF tantalum capacitor for decoupling and local charge storage.
8	VID4	**VID4 Input**. A logic 1 on this open collector/TTL input will enable the VID3–VID0 inputs to set the output from 2.1V to 3.5V, and a logic 0 will set the output from 1.3V to 2.05V, as shown in Table 1. Pullup resistors are internal to the controller.
9	LODRV	**Low Side FET Driver**. Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be < 0.5".
10, 11	GNDP	**Power Ground**. Return pin for high currents flowing in pins 7 and 13 (VCCP and VCCQP). Connect to a low impedance ground.
12	HIDRV	**High Side FET Driver**. Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be < 0.5".
13	VCCQP	**Power VCC**. This is the supply for the high side FET driver. VCCQP must be connected to a voltage of at least VCCA + $V_{GS,ON}$ (MOSFET).
14	GNDD	**Digital Ground**. Return path for digital logic. Connect to a low impedance system ground plane to minimize ground loops.
15	GNDA	**Analog Ground**. Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
16	VREF	**Reference Voltage Test point**. This pin provides access to the DAC output and should be decoupled to ground using 0.1µF capacitor. No load should be connected.
17-20	VID0-VID3	**Voltage Identification Code Inputs**. These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1. Pull-up resistors are internal to the controller.

Absolute Maximum Ratings

Supply Voltages, VCCA, VCCP, VCCQP	13V
Voltage Identification Code Inputs, VID4-VID0	13V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage, VCCA, VCCP		4.75	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temp		0		70	°C
Output Driver Supply, VCCQP		8.5		12	V
PWRGD threshold	Logic High Logic Low	93 88		107 112	$\%V_O$ $\%V_O$

Electrical Specifications

(V_{CCA} = 5V, V_{OUT} = 2.8V, f_{osc} = 300 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)
The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See Table 1	•	1.3		3.5	V
Output Current				13		A
Initial Voltage Setpoint	I_{LOAD} = 0.8A			±20		mV
Output Temperature Drift	T_A = 0 to 60°C	•		+10		mV
Load Regulation	I_{LOAD} = 0.8A to 15A	•		-25		mV
Line Regulation	V_{IN} = 4.75V to 5.25V	•		±2		mV
Output Ripple	20MHz BW, I_{LOAD} = 15A			±11		mV
Output Voltage Regulation Steady State[1] Transient[2]	 V_{OUT} = 2.8V, I_{LOAD} = 0 to 13A I_{LOAD} = 0.8 to 14.2A, 30A/µs	 • •	 2.74 2.67	 2.80 2.80	 2.90 2.93	 V V
Output Voltage Regulation Steady State[1] Transient[2]	See Note 3 V_{OUT} = 1.8V I_{LOAD} = 0.8 to 15A, 20A/µs	 • •	 1.74 1.70	 1.80 1.80	 1.86 1.90	 V V
Efficiency	I_{LOAD} = 13A, V_{OUT} = 2.8V	•	80	85		%
Output Driver Rise and Fall Time	See Figure 2			50		ns
Output Driver Nonoverlap Time	See Figure 2			50		ns
Turn-on Response Time	I_{LOAD} = 0A to 13A				10	ms
Oscillator Range			80	300	1000	KHz
Oscillator Frequency	C_{EXT} = 100 pF		270	300	330	KHz
Max Duty Cycle			90	95		%

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, DC load regulation, output ripple/noise and temperature drift.
2. These specifications assume a minimum of 20, 1µF ceramic capacitors are placed directly next to the CPU in order to provide adequate high-speed decoupling. For motherboard applications, the PCB layout must exhibit no more than 0.5mΩ parasitic resistance and 1nH parasitic inductance between the converter output and the CPU.
3. In order to satisfy the specified Output Voltage Regulation requirements for V_{OUT} = 1.8V at 15A for next generation processors, the output capacitors must exhibit no more than 7.0mΩ equivalent ESR for a motherboard application.

Preliminary Information

Table 1. Output Voltage Programming Codes

VID4	VID3	VID2	VID1	VID0	V_{OUT} to CPU
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	No CPU
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V

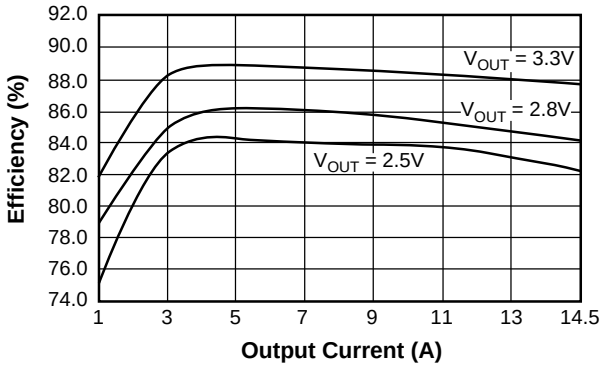
Note:

1. 0 = processor pin is tied to GND.
   1 = processor pin is open.

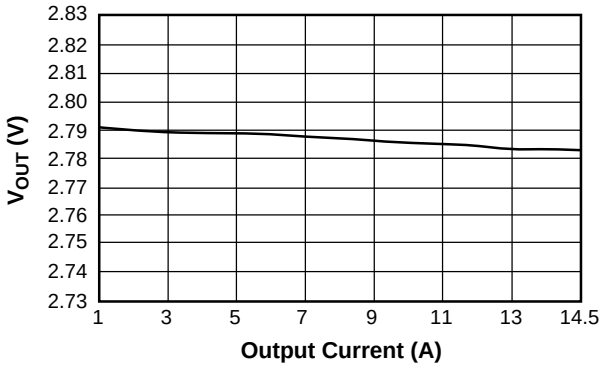
Typical Operating Characteristics

(VCCA, VCCD = 5V, fosc = 280 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)

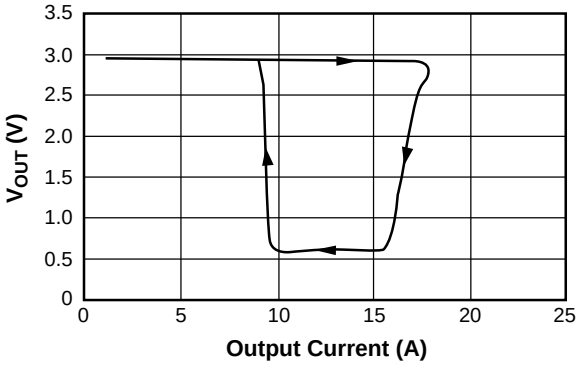
Efficiency vs. Output Current



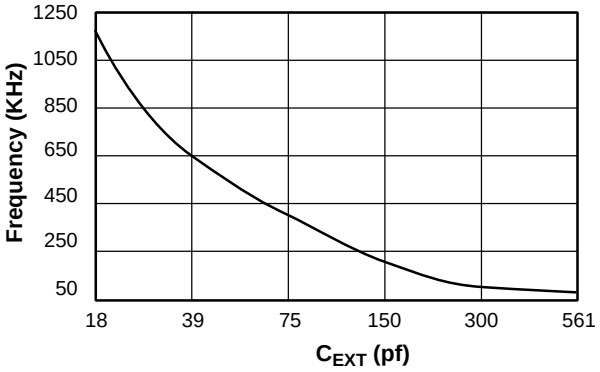
Load Regulation, V_{OUT} = 2.8 V



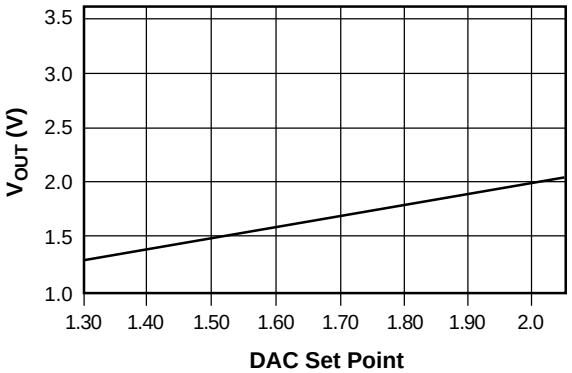
Output Voltage vs. Output Current, R_{SENSE} = 6mΩ



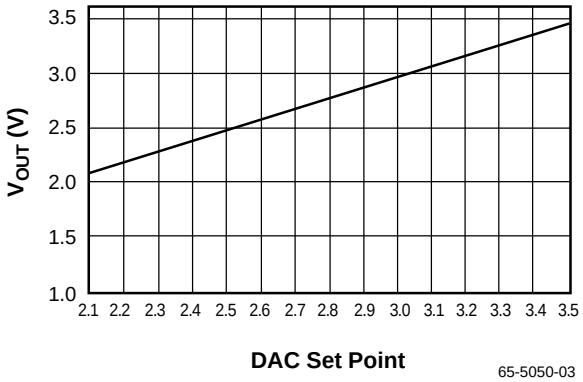
Oscillator Frequency vs. C_{EXT}



Output Programming, VID4 = 0



Output Programming, VID4 = 1



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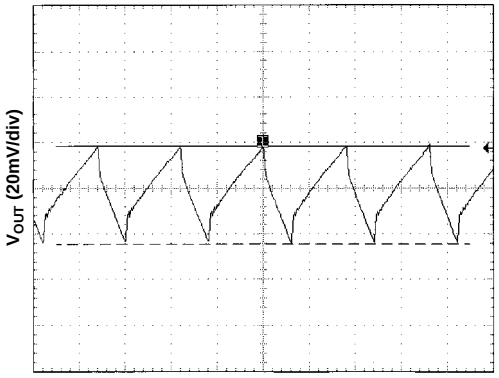
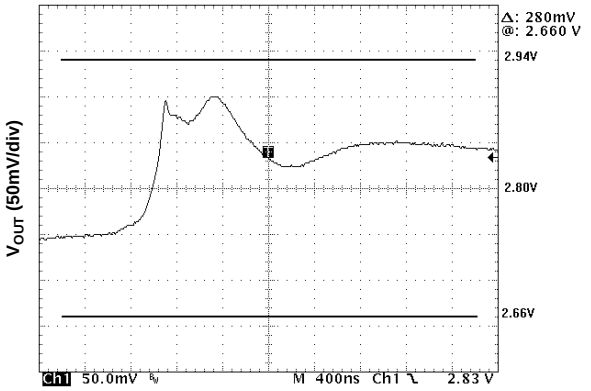
Typical Operating Characteristics (continued)

Output Ripple, 2.8V @ 13A



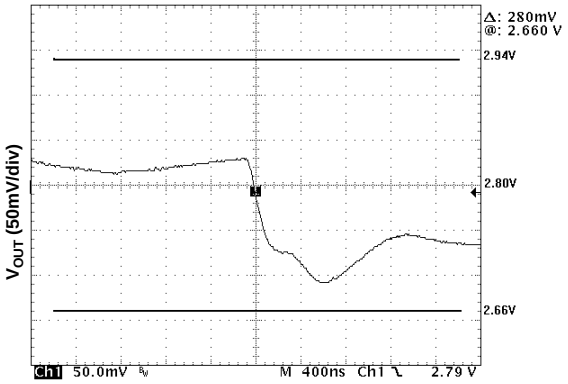
Time (2µs/division)

Transient Response, 13A to 0.5A



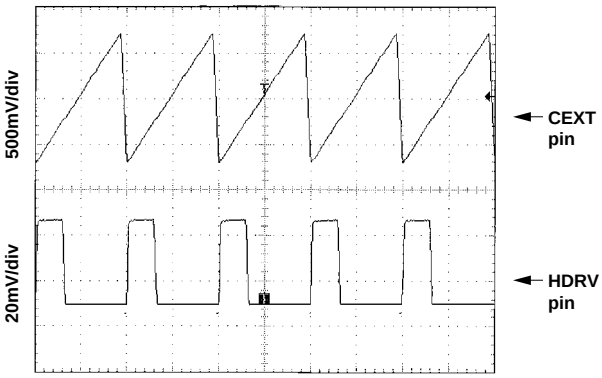
Time (400ns/division)

Transient Response, 0.5A to 13A



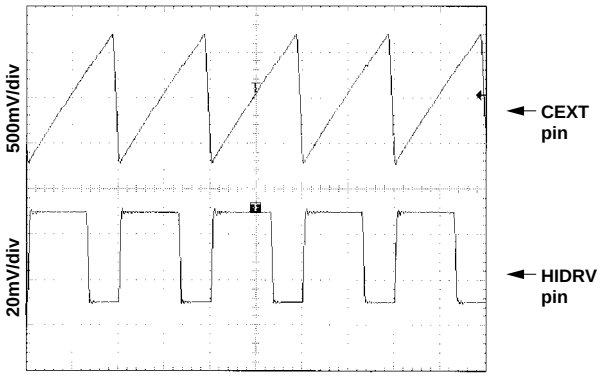
Time (400ns/division)

Switching Waveforms, 0.5A Load



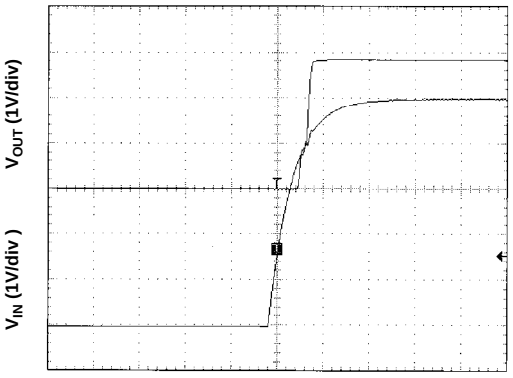
Time (2µs/division)

Switching Waveforms, 13A Load



Time (2µs/division)

Output Startup, System Power-up



Time (10ms/division)

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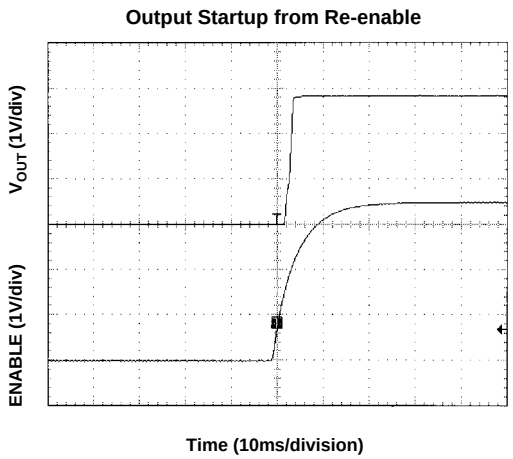
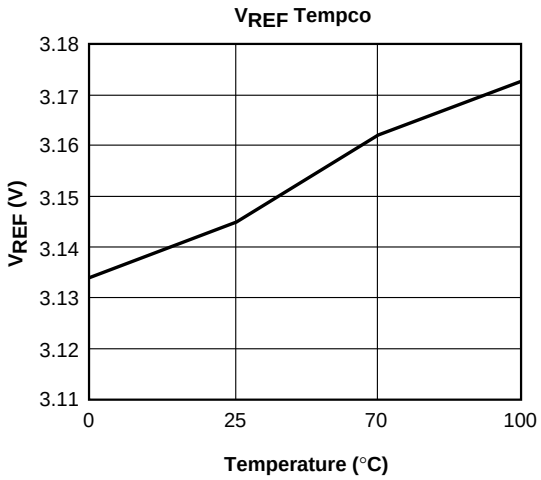
Typical Operating Characteristics (continued)





Test Circuits

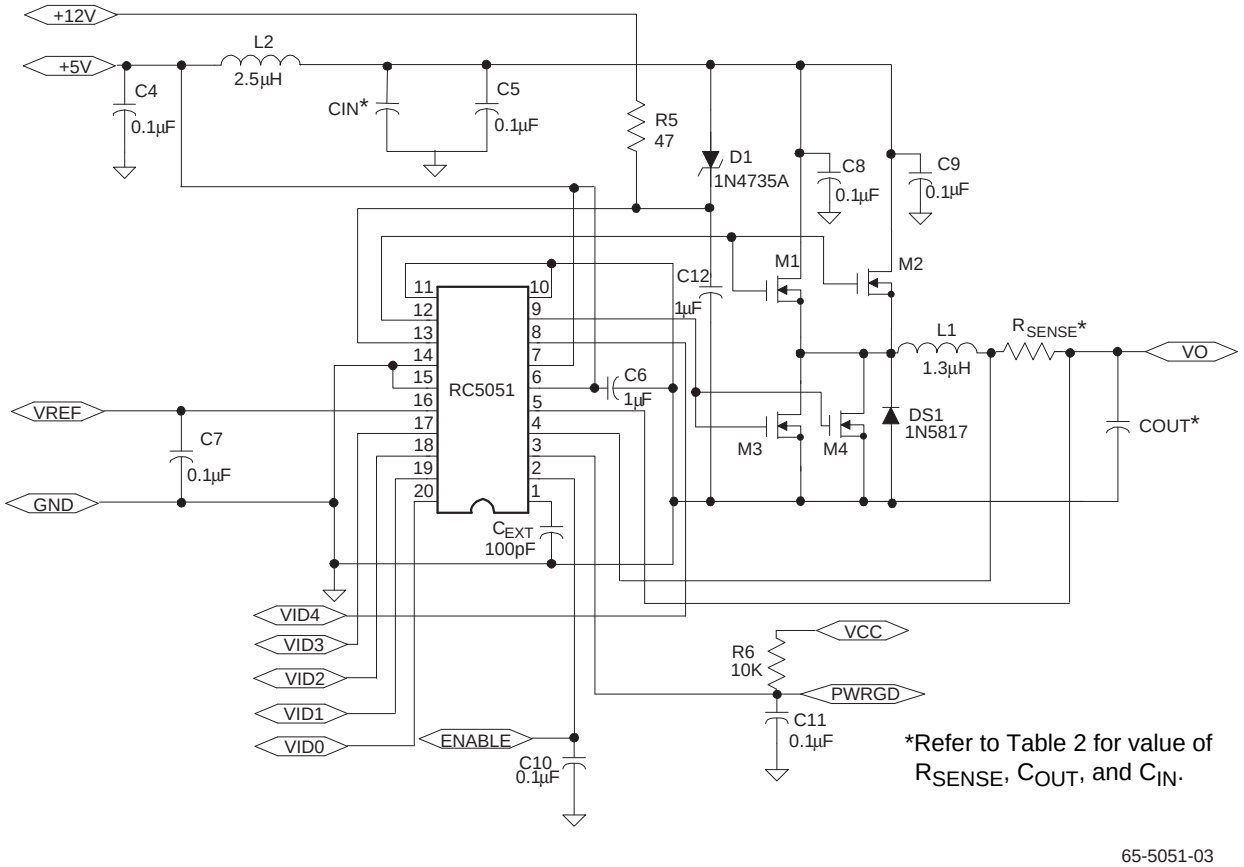


Figure 1. 15A Application Circuit for Pentium II Processor

Preliminary Information

Test Circuits (continued)

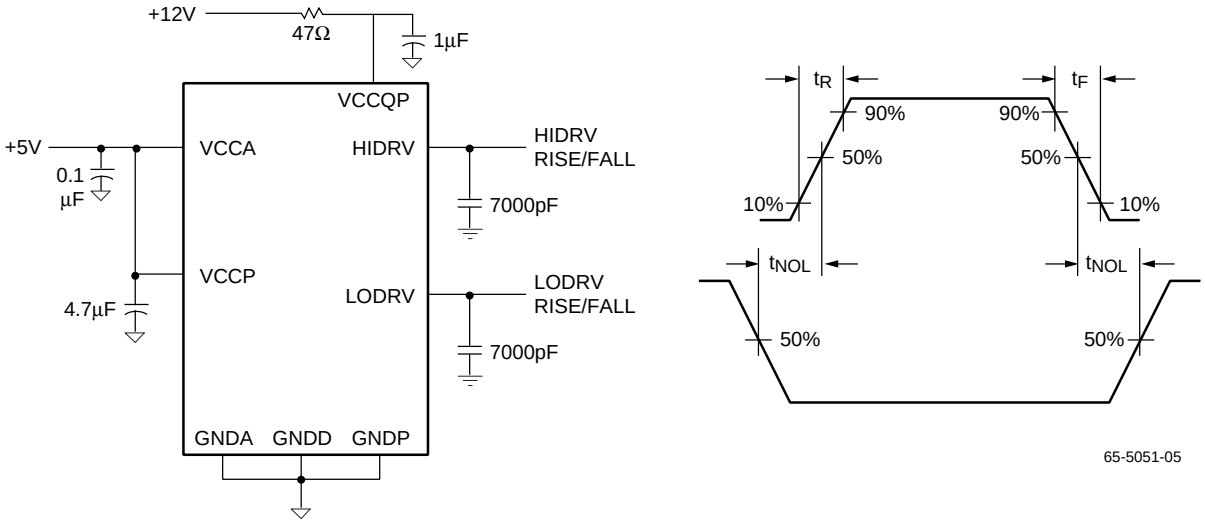


Figure 2. Output Drive Test Circuit

Table 2. Recommended Bulk Capacitors for CPU-based Applications

Application	Output Current	C_{IN}	C_{OUT}	C_{OUT} Maximum ESR	R_{SENSE}
Motorola PowerPC 603/604 Motherboard	7A	2 x 1500µF, 6V Sanyo 6MV1500CX	2 x 1500µF, 6V Sanyo 6MV1500SX	22mΩ	10.5mΩ
Intel Pentium II Klamath Motherboard	14.2	3 x 1200µF, 10V Sayno 10MV1200EG	5 x 1500µF, 6.3V Sanyo 6MV1500GX	9.0mΩ	6.0mΩ
Intel Pentium II Motherboard (All versions including next generation)	15A	3 x 1200µF, 10V Sayno 10MV1200EG	6 x 1500µF, 6.3V Sanyo 6MV1500GX	7.5mΩ	6.0mΩ

Preliminary Information

Table 3. RC5051 Application Bill of Materials for Intel Klamath Processor

Reference	Manufacturer Part #	Description	Requirements/Comments
C4, C5, C7–C11	Panasonic ECU-V1H104ZFX	0.1µF 50V capacitor	
Cext	Panasonic ECU-V1H121JCG	100pF capacitor	
C12, C6	Panasonic ECSH1CY105R	1µF 16V capacitor	
C_{IN}	United Chemi-con LXF16VB102M10X20LL	1000µF 10V electrolytic capacitor 10mm x 20mm	ESR < 62mΩ See Note 1 and Table 2
C_{OUT}	Sanyo 6MV1500GX	1500µF 6.3V electrolytic capacitor 10mm x 20mm	ESR < 44mΩ See Note 1 and Table 2
DS1	General Instrument 1N5817	Schottky Diode	3A, 20V
D1	1N4735A	6.2V Zener Diode, Motorola	
L1	Skynet 320-8107	1.3µH, 14A inductor DCR ~ 2.5mΩ	See Note 2
L2	Skynet 320-6110	2.5µH, 11A inductor DCR ~ 6mΩ	See Note 3
M1, M2, M3, M4	International Rectifier IRL3103	N-Channel Logic Level Enhancement Mode MOSFET	$R_{DS(ON)}$ < 19mΩ V_{GS} < 4.5V, I_D = 15A See Note 4
R_{SENSE}	Copel AWG#18	5.5mΩ CuNi Alloy Wire Resistor	
R5	Panasonic ERJ-6GEY050Y	47Ω 5% resistor	
R6	Panasonic ERJ-6ENF10.0KV	10KΩ 5% resistor	

Notes:

1. In order to meet the voltage transient requirements for the Intel Pentium II Motherboard application, the equivalent ESR of the output capacitors must not exceed 7.5mΩ. In order to satisfy the specified Output Voltage Regulation requirements for V_{OUT} = 1.8V at 15A for next generation processors, the output capacitors must exhibit no more than 7.0mΩ equivalent ESR for a motherboard application. The use of the capacitors recommended in Table 1 will address this and other voltage specifications without significant added cost, although it is left up to the user to specify the components used. Please refer to Application Bulletin 5 for additional considerations required to meet the Intel Pentium II voltage transient specifications.
2. To optimize a converter for 15A at 1.8V output, f_{SW} = 300 kHz, change the value of L1 to 1.24µH.
3. Inductor L2 is recommended to isolate the 5V input supply from current surges caused by MOSFET switching. L2 is not required for normal operation and may be omitted if desired.
4. For 15A designs using IR3103 MOSFETs, heat sinks with thermal resistance Θ_{SA} < 50°C/W should be used.

Preliminary Information

Application Information

The RC5051 Controller

The RC5051 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the RC5051 can be configured to deliver more than 15A of output current. The RC5051 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the RC5051 Block Diagram on page 1. The control loop of the regulator contains two main sections; the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital control block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The voltage control path amplifies the VFB signal and presents the output to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The additional comparators in the analog control section set the point at which the RC5051 enters its pulse skipping mode during light loads as well as the point at which the current limit comparator disables the output drive signals to the external power MOSFETs.

The digital control block takes the comparator inputs and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs. The digital utilizes high speed Schottky transistor logic, allowing the RC5051 to operate at clock speeds as high as 1MHz.

High Current Output Drivers

The RC5051 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. Each driver's power and ground are separated from the chip's power and ground for additional switching noise immunity. The HIDRV driver has a power supply, VCCQP, which is supplied from an external 12V source through a series resistor or a charge-pump circuit powered from 5V if 12V is not available. The resulting voltage is sufficient to provide the gate to source drive to the external MOSFET required in order to achieve a low $R_{DS,ON}$. Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage and its VCCP power pin can be tied to VCC.

Internal Voltage Reference

The reference included in the RC5051 is a precision bandgap voltage reference. The internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Added to the reference input is the resulting output from an integrated 5-bit DAC. The 5-bit DAC monitors the 4 voltage identification pins, VID0–VID3, as well as a range select pin (RSEL). When the RSEL pin is at logic HIGH, the DAC will scale the reference voltage from 2.0V to 3.5V in 100mV increments. When RSEL is pulled LOW, the DAC will scale the reference from 1.30V to 2.05V in 50mV increments. For guaranteed stable operation under all loading conditions, 0.1µF of decoupling capacitance should be connected to the VREF pin. No load should be connected to VREF.

Power Good (PWRGD)

The RC5051 Power Good function is designed in accordance with the Pentium II DC-DC converter specifications and provides a constant voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage exceed ±12% of its nominal setpoint. The Power Good flag provides no other control function to the RC5051.

Output Enable (ENABLE)

The RC5051 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Upgrade Present (UP#)

Intel specifications state that the DC-DC converter should accept an open collector signal, used to indicate the presence of an upgrade processor. The typical state is high (that is, a standard process is in the system). When in the low or ground state (an OverDrive processor is present), the output voltage must be disabled unless the converter can supply the requirements of the OverDrive processor. When disabled, the PWRGD output must be in the low state. The RC5051 can supply the requirements of the OverDrive processor, the UP# signal is not required.

Over-Voltage Protection

The RC5051 constantly monitors the output voltage for protection against over voltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an over-voltage condition is assumed and the RC5051 disables the output drive signal to the external MOSFETs.

Short Circuit Protection

A current sense methodology is implemented to disable the output drive signal to the MOSFETs when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When the voltage developed across the sense resistor exceeds the 120mV comparator threshold voltage, the RC5051 reduces the output duty cycle to protect the power devices.

The DC-DC converter returns to normal operation after the fault has been removed, for either an overvoltage or a short circuit condition.

Oscillator

The RC5051 oscillator section uses a fixed current capacitor charging configuration. An external capacitor (C_{EXT}) is used to preset the oscillator frequency between 80KHz and 1MHz. This scheme allows maximum flexibility in setting the switching frequency and in choosing external components.

In general, a lower operating frequency decreases the peak ripple current flowing in the output inductor, thus allowing the use of a smaller inductor value. Unfortunately, operation at lower frequencies increases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to slower loop response of the controller.

In addition, the efficiency losses due to switching of the MOSFETs increase as the operating frequency is increased. Thus, efficiency is optimized at lower frequencies. An operating frequency of 300KHz was chosen to optimize efficiency while maintaining excellent regulation and transient performance under all operating conditions.

Design Considerations and Component Selection

MOSFET Selection

This application requires N-channel *Logic Level* Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON}$ < 20mΩ (lower is better)
- Low gate drive voltage, $V_{GS} \leq 4.5V$
- Power package with low Thermal Resistance
- Drain-Source voltage rating > 15V

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter.

MOSFET Gate Bias

The high side MOSFET gate driver can be biased by one of two methods—Charge Pump or 12V Gate Bias. The charge pump method has the advantage of requiring only a single input voltage, but the 12V method will realize increased efficiency by providing an increased average V_{GS} to the high side MOSFETs.

Method 1. Charge Pump (Bootstrap)

Figure 3 employs a charge pump to provide gate bias. Capacitor CP is the charge pump deployed to boost the voltage of the RC5051 output driver. When the MOSFET switches off, the source of the MOSFET is at -0.6V. VCCQP is charged through the Schottky diode to 4.5V. Thus, the capacitor CP is charged to 5V. When the MOSFET turns on, the source of the MOSFET voltage is equal to 5V. The capacitor voltage follows, and hence provides a voltage at VCCQP equal to 10V. The Schottky diode is required to provide the charge path when the MOSFET is off, and reverses bias when VCCQP goes to 10V. The charge pump capacitor (CP) needs to be a high Q, high frequency capacitor. A 1µF ceramic capacitor is recommended here.

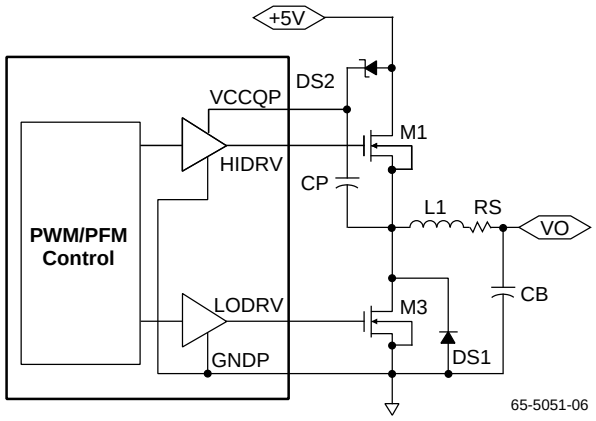


Figure 3. Charge Pump Configuration

Method 2. 12V Gate Bias

Figure 4 illustrates how a 12V source can be used to bias VCCQP. A 47Ω resistor is used to limit the transient current into the VCCQP pin and a 1µF capacitor is used to filter the VCCQP supply. This method provides a higher gate bias voltage (V_{GS}) to the MOSFETs, and therefore reduces the effective $R_{DS,ON}$ and the resulting power loss within the MOSFET. In designs where efficiency is a primary concern, the 12V gate bias method is recommended. A 6.2V Zener diode, D1, is used to clamp the voltage at VCCQP to a maximum of 12V and ensure that the absolute maximum voltage of the IC will not be exceeded.

Preliminary Information

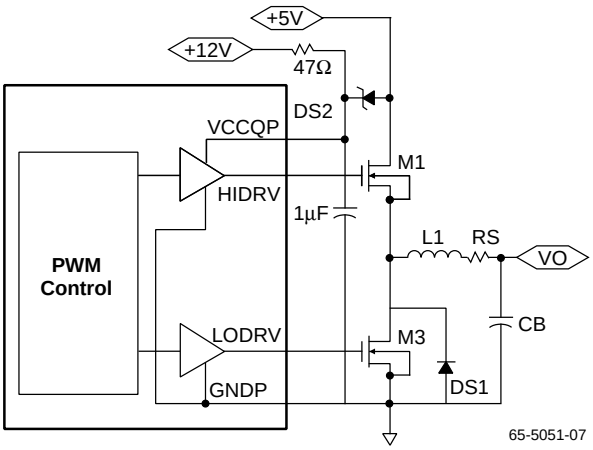


Figure 4. 12V Gate Bias Configuration

Choosing the value of the inductor is a tradeoff between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed range in order to maximize either ripple or transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{OUT} - V_{IN})}{f} \times \frac{V_{OUT}}{V_{IN}} \times \frac{ESR}{V_r}$$

where:

- V_{IN} = Input Power Supply
- V_{OUT} = Output Voltage
- f = DC/DC converter switching frequency
- ESR = Equivalent series resistance of all output capacitors in parallel
- V_r = Peak to peak output ripple voltage budget

The first order equation for maximum allowed inductance is:

$$L_{min} = 2Co \times \frac{(V_{IN} - V_{OUT})D_m V_{tb}}{I_{p^2}}$$

where:

- Co = The total output capacitance
- I_p = Peak to peak load transient current
- V_{tb} = The output voltage tolerance budget allocated to load transient
- D_m = Maximum duty cycle for the DC/DC converter (usually 95%)

Some margin should be maintained between L_{min} and L_{max}. Adding margin by increasing L_{max} almost always adds expense since all the variables are predetermined by system performance except for C_o, which must be increased to increase L_{max}. Adding margin by decreasing L_{min} can either be done by purchasing capacitors with lower ESR or by increasing the DC/DC converter switching frequency. The RC5051 is capable of running at high switching frequencies and provides significant cost savings for the newer CPU systems that typically run at high supply current.

RC5051 Short Circuit Current Characteristics

The RC5051 short circuit current characteristic includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. Figure 5 shows the typical characteristic of the DC-DC converter circuit with a 6 mΩ sense resistor. The converter exhibits a normal load regulation characteristic until the voltage across the resistor exceeds the internal short circuit threshold of 120mV. At this point, the internal comparator trips and signals the controller to reduce the converter's duty cycle to approximately 20%. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe operating range for the DC-DC converter.

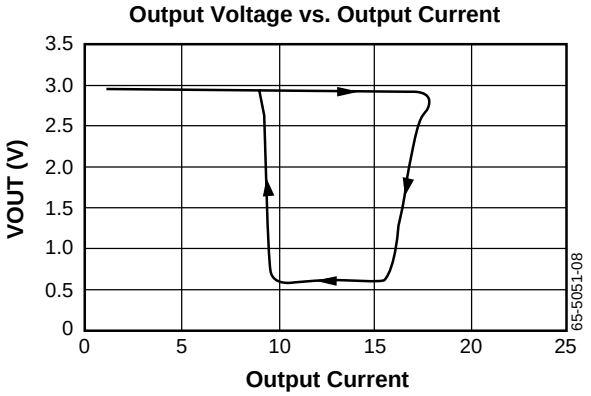


Figure 5. RC5051 Short Circuit Characteristic

Schottky Diode Selection

The application circuits of Figures 1 and 2 show a Schottky diode, DS1, which is used as a free-wheeling diode to assure that the body-diodes in M3 and M4 do not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for these diodes to conduct because their high forward voltage drop degrades efficiency. Since this time duration is very short, a 3A Schottky diode will suffice for this application.

Output Filter Capacitors

Output ripple performance and transient response are functions of the filter capacitors. Since the 5V supply of a PC motherboard may be located several inches away from the DC-DC converter, the input capacitance can play an important role in the load transient response of the RC5051. The higher the input capacitance, the more charge storage is available for improving the current transfer through the FETs. Low Equivalent Series Resistance (ESR) capacitors are best suited for this type of application. Incorrect selection can hinder the converter's overall performance. The input capacitors should be placed as close to the drain of the FET as possible to reduce the effect of ringing caused by long trace lengths.

The ESR rating of a capacitor is a difficult number to quantify. ESR is defined as the resonant impedance of the capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for this device to have a resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained using the following equation:

$$ESR = \frac{DF}{2\pi fC}$$

Where DF is the dissipation factor of the capacitor, f is the operating frequency, and C is the capacitance in farads.

With this in mind, correct calculation of the output capacitance is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple and load transient response. The calculation is as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR}$$

Where ΔV is the maximum voltage deviation due to load transients, ΔT is the reaction time of the power source (Loop response time of the RC5051 is approximately 2µs), and I_O is the load current step.

For I_O = 14.2A (0.8–15A load step) and ΔV= 110mV, the bulk capacitance required can be approximated as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR} = \frac{14.2A \times 2\mu s}{110mV - 14.2A \times 7.0m\Omega} = 2180\mu F$$

Because the control loop response of the controller is not instantaneous, the initial load transient must be supplied entirely by the output capacitors. The initial voltage deviation will be determined by the total ESR of the capacitors used and the parasitic resistance of the output traces. For a detailed analysis of capacitor requirements in a high-end microprocessor system, please refer to Application Bulletin AB-5.

Input Filter

The DC-DC converter design should include an input inductor between the system +5V supply and the converter input as described below. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of 2.5µH is recommended.

The recommended 3 x 100µF capacitors deliver current when the high side MOSFET switches on.

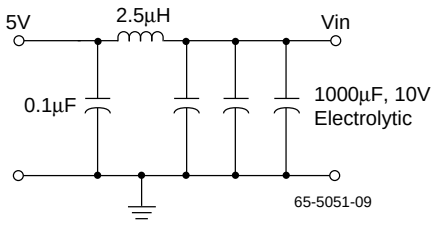


Figure 6. Input Filter

PCB Layout Guidelines

- Placement of the MOSFETs relative to the RC5051 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the RC5051 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the RC5051. That is, traces that connect to pins 9, 12, and 13 (LODRV, HIDRV and VCCQP) should be kept far away from the traces that connect to pins 1 through 5, and pin 16.
- Place the 0.1µF decoupling capacitors as close to the RC5051 pins as possible. Extra lead length on these negates their ability to suppress noise.
- Each VCC and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Surround the CEXT timing capacitor with a ground trace. Be sure to place a ground or power plane underneath the capacitor for further noise isolation to provide additional shielding to the oscillator (pin 1) from the noise on the PCB. In addition, place this capacitor as close to pin 1 as possible.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in #1 above. Place the input bulk capacitors as close to the drains of MOSFETs as possible. In addition, placement of a 0.1µF decoupling cap right on the drain of each MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.

- The traces that run from the RC5051 IFB (pin 4) and VFB (pin 5) pins should be run together next to each other and Kelvin connected to the sense resistor. Running these lines together rejects some of the common mode noise that is presented to the RC5051 feedback input. Try, as much as possible, to run the noisy switching signals (HIDRV, LODRV & VCCQP) on one layer, but use the inner layers for power and ground only. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing signals VFB and IFB.

PC Board Layout Checklist

- **Bypass Capacitor near Vref pin.**
  This pin should be adequately bypassed with a 0.1µF capacitor.
- **Bypass Capacitors for VCC (5V).**
  A 0.1µF should be placed right next to the VCC pin of the controller.
- **Bypass Capacitors for Power MOSFET.**
  A 0.1µF cap should be placed at the drain connection of each power MOSFET.
- **5V Connection to the controller IC.**
  Each VCC pin on the IC should be connected to the 5V power plane through its own via.
- **Power MOSFET Gate Drive Trace.**
  - The gate drive trace should be routed on one layer only.
  - The controller IC and the power FET should be oriented in such a way as to minimize the trace length of the gate drive trace (< 1 inch).
  - The gate drive trace routing should stay away from the quiet analog section of the RC50XX controller IC. (i.e. keep away from Vref, IFB, VFB, and CEXT.)
- **Bulk Capacitance.**
  - The input bulk capacitance needs to be located less than 1" from the drain of the power MOSFET. We recommend the following guidelines for the amount of bulk input capacitance:
    - For an output load of <10A use 2 X 1500µF caps.
    - For an output load of >10A use 3 X 1500µF caps.
  - The output bulk capacitors should be located as close to the CPU socket as possible. We recommend the following guidelines for the amount of bulk output capacitance:
    - For Pentium Pro use 4 X 1500µF.
    - For P55C MMX Pentium/ AMD K6 use 2X 1500µF.
    - For Pentium II use 7 X 1500µF.
- **Inductor Location.**
  The inductor should be located near to the Source of the Power MOSFET. The ideal condition would be to use an internal power plane to connect the Source of the power MOSFET, the inductor, and the flyback schottky diode together.
- **Sense Resistor.**
  - The sense resistor should be located next to the inductor.
  - The two traces that run from the sense resistor to the RC50XX controller IC should be minimum width traces and be run parallel to each other. We recommend these sense resistor values:
    - For Pentium Pro use 0.006Ω.
    - For P55C MMX Pentium/ AMD K6 use 0.007Ω.
    - For Pentium II use 0.006Ω.
- **Ground Plane.**
  The RC50XX controller IC have a continuous ground plane running underneath the entire chip area. Each of the IC ground pins should have a separate via connection down into the ground plane.
- **Input Filter.**
  In many high current DC-DC converter designs, it is advisable to add an input inductor in order to create an input filter. An inductor on the order of 1-3uH is usually all that is required to perform the filter. When this component is added to the circuit, it is important that the RC50XX controller IC receive its VCC power from the system side of the input inductor and not the “dirty” side of the inductor. (ie the side that is connected to the power MOSFET drains)
- **To Minimize Electromagnetic Interference (EMI).**
  - Avoid long ground connections. Connect directly to the ground plane.
  - Use a star ground, where all grounds are connected to one point.
  - Use good quality inductors such as torrids or pot cores. Avoid rod inductors.
  - Route the high current carrying traces as power planes where possible.
  - Keep sensitive low-level signals away from the active switching components. Try to route them using the ground plane as a shield.

PC Motherboard Sample Layout and Gerber File

A reference design for motherboard implementation of the RC5051 along with the PCAD layout Gerber file and silk screen can be obtained from our marketing department at 415-966-7734.

RC5051 Evaluation Board

Raytheon provides an evaluation board to verify the system level performance of the RC5051. It serves as a guide to performance expectations when using the supplied external components and PCB layout. Please call the marketing department at 415-966-7734 for an evaluation board.

Additional Information

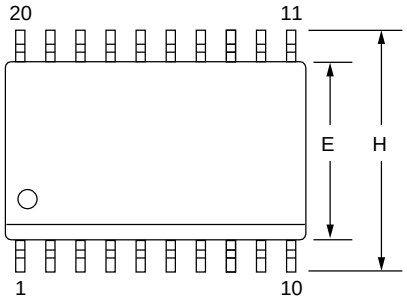
For additional information contact the Raytheon Electronics Semiconductor Division marketing at 415-966-7734.

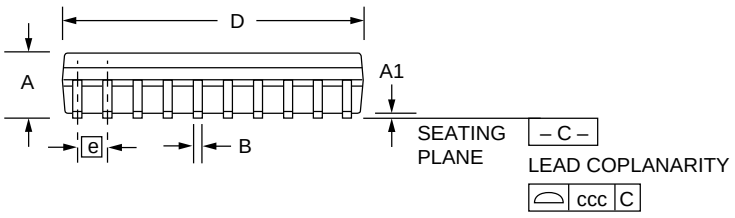
Mechanical Dimensions – 20 Lead SOIC

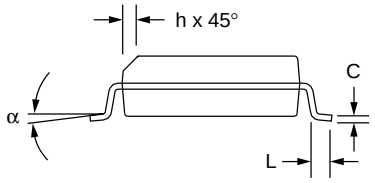
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC5051M	20 pin SOIC

Preliminary Information

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